**IN THE SPECIFICATION:**

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**Please substitute the following paragraph for the paragraph beginning at line 5:**

The viewpoint of sharing the substrate potential may be also grasped from the viewpoint of sharing the well region in the MIS transistor. A semiconductor integrated circuit has: a first logic gate (1) using, as an operation power source, a first pair of potentials (VDDL and VSSL, VDDL and VSS) having a relatively small potential difference; and a second logic gate (2) using, as an operation power source, a second pair of potentials (VDDH and VSSH, VDDH and VSS) having a relatively large potential difference. Each of the first and second logic gates has an MIS transistor, a well region (NWELL, PWELL) in which an MIS transistor of the first logic gate is formed and a well region (NWELL, PWELL) in which an MIS transistor of the second logic gate is formed are made common every conduction type. According to the potential applied to the well region in the MIS transistor, the bias state of the MIS transistor is determined. The action at this time is the same as the above 1.

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**Please substitute the following paragraph for the paragraph beginning at line 12:**

Specific modes of the pair of the first and second potentials and the substrate potential are as follows. As a first mode, as shown in Fig. 1, the first potential pair includes a first high potential (VDDL) and a first low potential (VSSL), the second potential pair includes a second high potential (VDDH) higher than the first high potential and a second low potential (VSSH) lower than the first low potential, and the substrate potentials include a high potential side substrate potential (VBP) between the first and second high potentials and a low potential side substrate potential (VBN) between the first and second low potentials. In the mode, as described above, the reverse substrate bias state is achieved in both of the p-channel type MIS transistor and the n-channel type MIS transistor included in the first logic gate, and the forward substrate bias state is achieved in both of the p-channel type MIS transistor and the n-channel type MIS transistor included in the second logic gate.

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**Please substitute the following paragraph for the paragraph beginning at line 19:**

Figs. 19A and 19B schematically show power lines in a cell. Fig. 19A shows an example of a conventional cell layout having a pair of a power line interconnection and a ground line in a cell. Shown in Fig. 19A are a metal line 40 for transmitting the substrate potential VBP of a pMOS transistor, a metal line 41 for transmitting the power source potential VDD, a metal line 42 for transmitting the power source potential VSS, and a metal line 43 for transmitting the substrate potential VBN of an nMOS transistor. Fig. 19B shows an example of a layout of a cell such as a high-speed cell or low-power cell according to the invention. Shown in Fig. 19B are a metal line 44 for transmitting the substrate potential VBP of a pMOS transistor, a metal line 45 for transmitting a power source potential VDDH, a metal line 46 for transmitting the power source potential VDDL, a metal line 47 for transmitting the power source potential VSSL, a metal line 48 for transmitting the power source potential VSSH, and a metal line 49 for transmitting the substrate potential VBN of the nMOS transistor. In the case of a high-speed cell, the source of a MOS transistor is connected to the metal lines 45 and 48. In the case of a low-power cell, the source of a

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MOS transistor is connected to the metal lines 46 and 47. By using a layout in which a plurality of power lines are arranged in a single cell as described above, the layout in which high-speed cells and low-power cells mixedly exist as shown in Fig. 17 is simplified. With respect to the width of the power line 41 in the conventional example of Fig. 19A and that of the power lines 45 and 46 in the layout according to the invention of Fig. 19B, since the invention provides the function of decreasing the power consumption of a circuit as described above, it is unnecessary to make the total of the widths of the power lines 45 and 46 wider than the width of the power line 41. Therefore, the cell size according to the layout of the invention does not become larger than that according to the conventional layout.

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